ABSTRACT OF THE DISCLOSURE

A reconfigurable channel CODEC (encoder and decoder) processor for a wireless communication system is disclosed. A high degree of user programmability and reconfigurability is provided by the channel CODEC processor. In particular, the reconfigurable channel CODEC processor includes processor cores and algorithm-specific kernels that contain logic circuits tailored for carrying out predetermined but user-configurable decoding and encoding algorithms. The interconnects between the processor cores and the algorithm-specific kernels are also user-configurable. Thus, the same hardware can be reconfigured for many different wireless communication standards.